

Figure 1

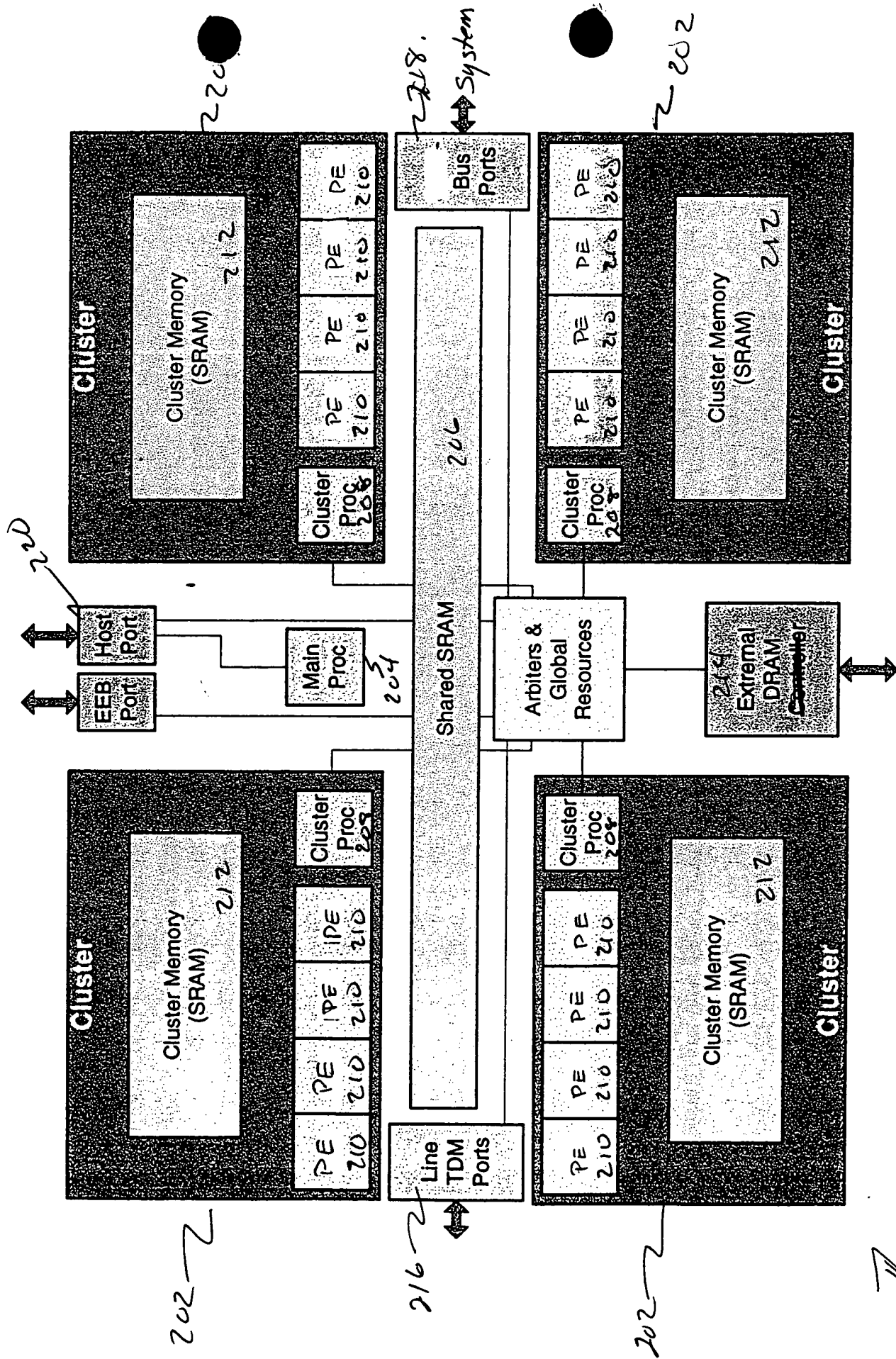


Figure 2

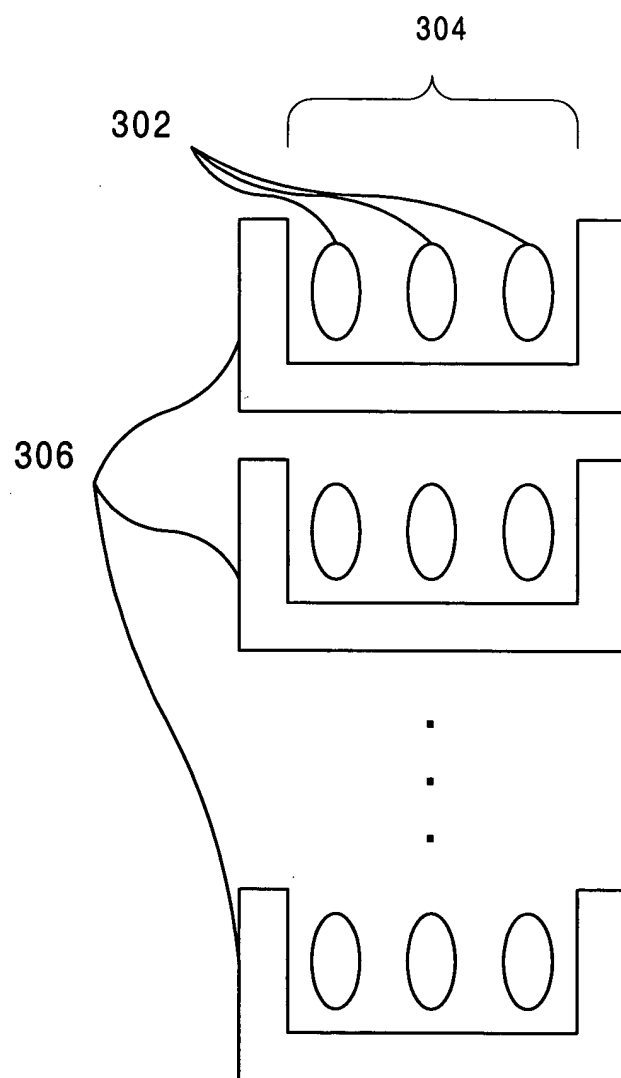


Figure 3

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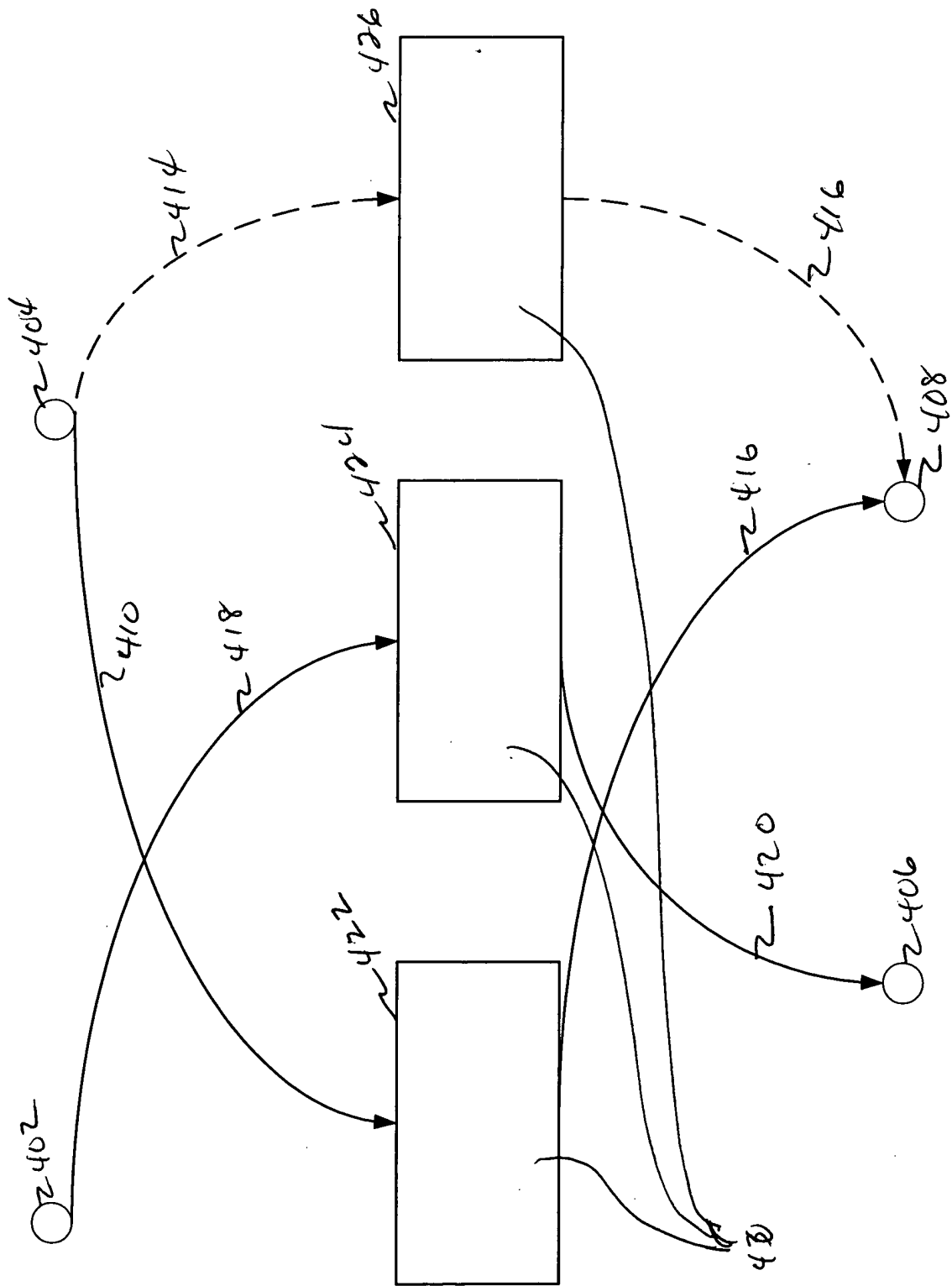


Figure 4

500

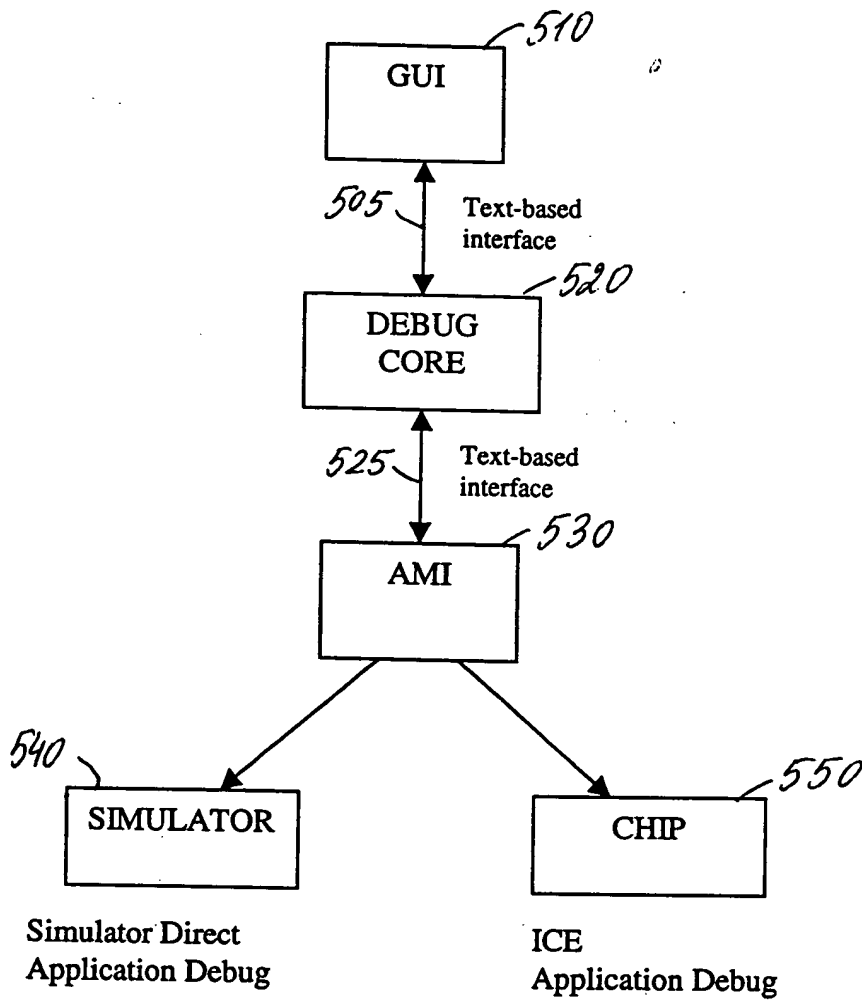


FIGURE 5A

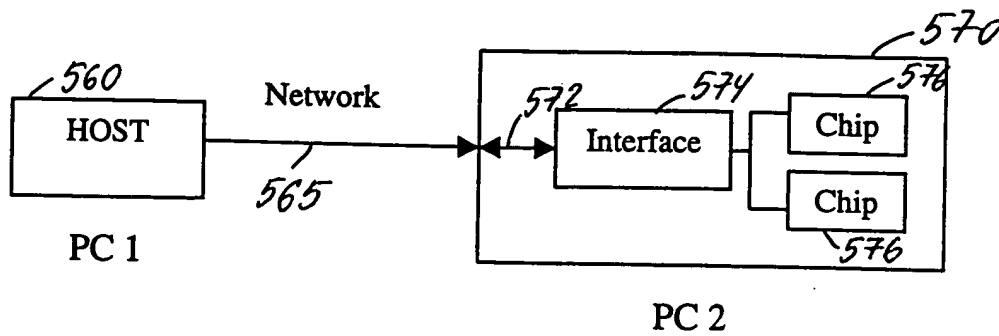


FIGURE 5B

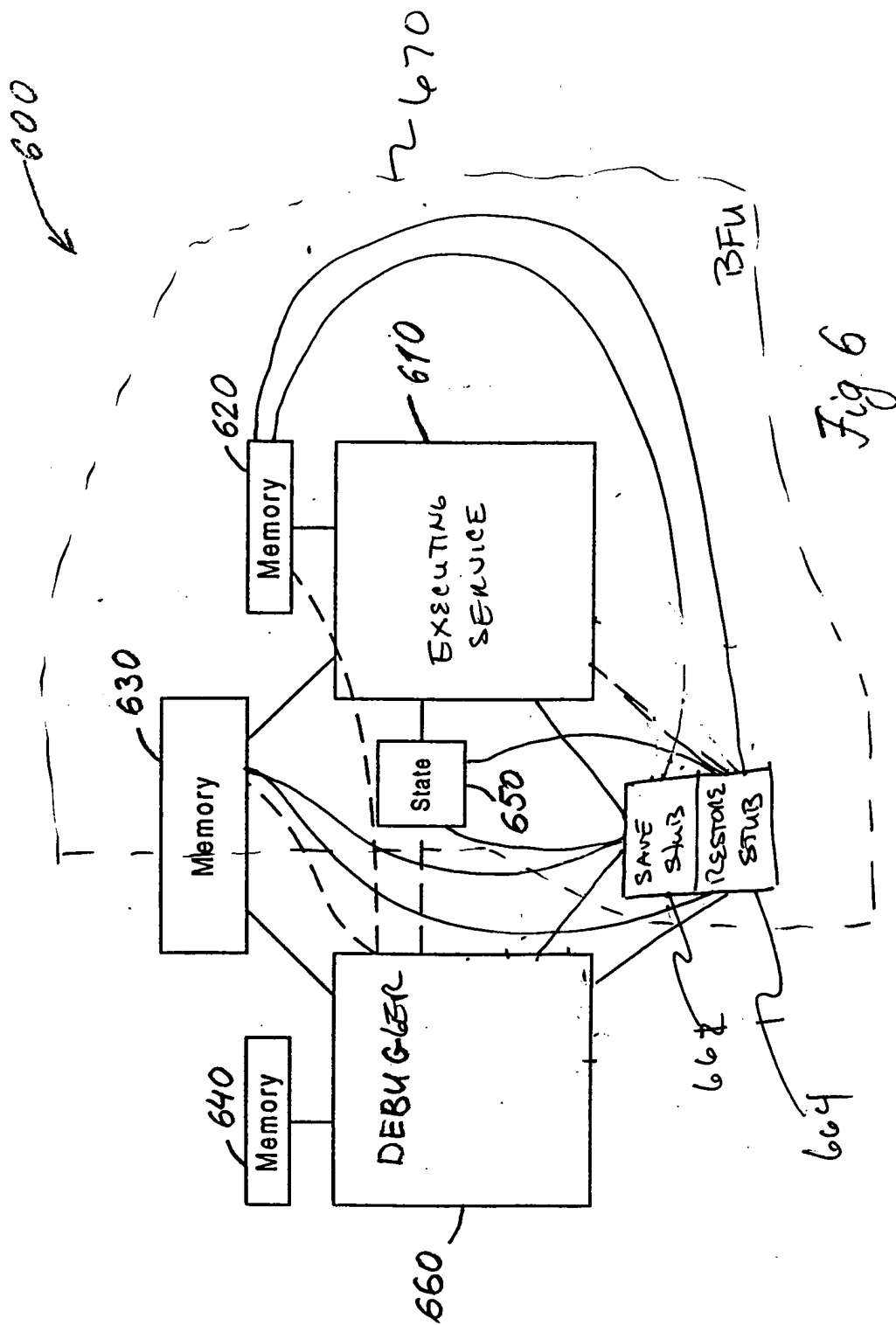


Fig 6

1	ld32 r3, (r1 + 0)
2	ld32 r4, (r1 + 4)
3	ld32 r5, (r1 + 8)
4	add r6, r3, r4

## Figure 7

1	ld32 r3, (r1 + 0)
2	ld32 r3, (r1 + 4)
3	ld32 r3, (r1 + 8)
4	ld32 r3, (r1 + 12)
5	st32 (r1 + 0), r3
6	st32 (r1 + 4), r3
7	st32 (r1 + 8), r3
8	st32 (r1 + 12), r3

## Figure 8

1	ld32 r3, (r1 + 0)
2	ld32 r4, (r1 + 0)
3	ld32 r5, (r1 + 0)
4	ld32 r6, (r1 + 0)
5	add r7, r5, r6

## Figure 9

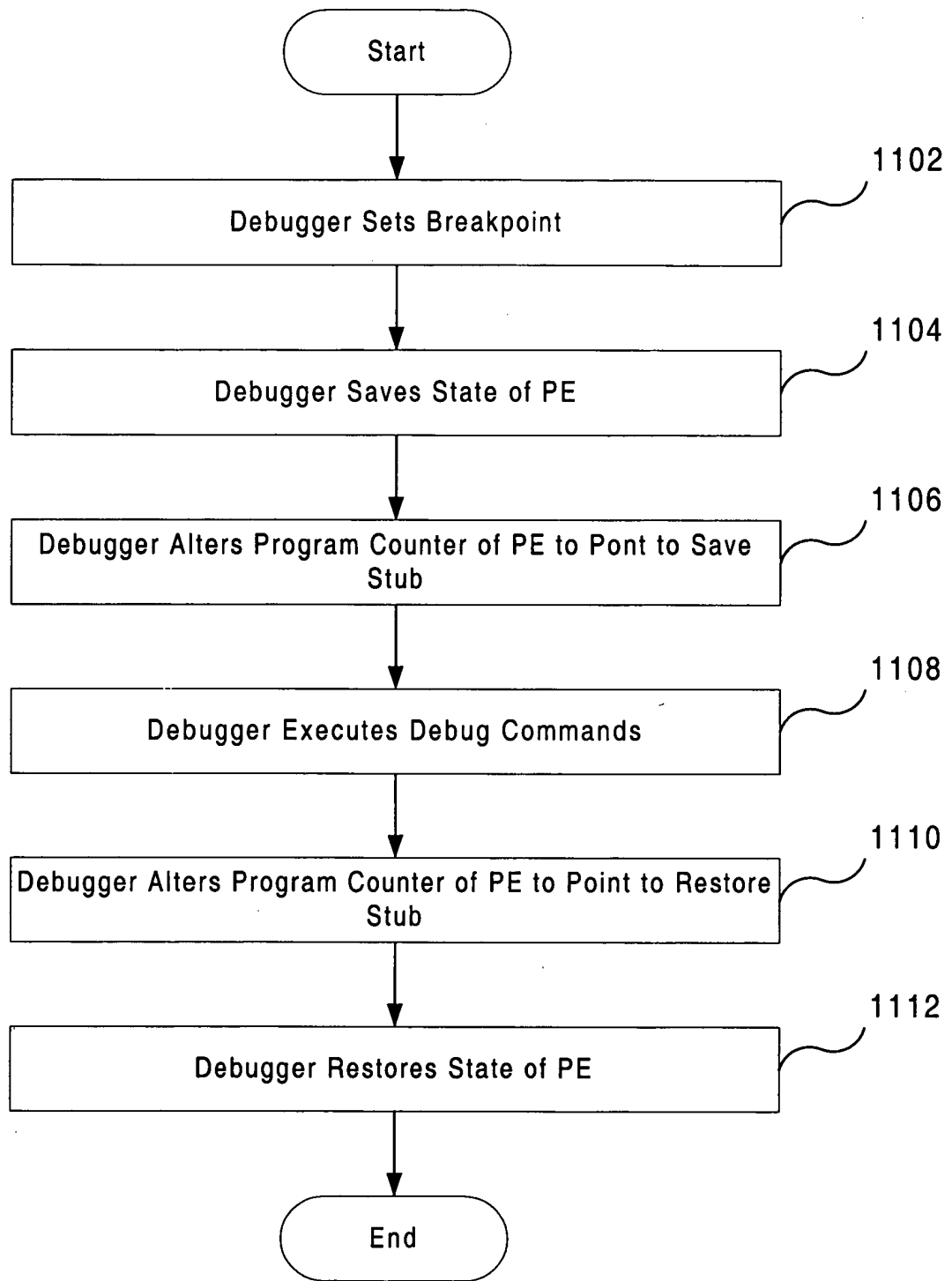
0000 0000 0000 0000

Scaler Registers	1002
Predicate Registers	1004
Vector Registers	1006
Least Significant 32-bits of Accumulator 0	1008
Most Significant 8-bits of Accumulator 0	1010
Least Significant 32-bits of Accumulator 1	1012
Most Significant 8-bits of Accumulator 1	1014
Least Significant 32-bits of Multiplier Output Register	1016
Most Significant 1-bit of Multiplier Output Register	1018
Loop Count Value (lcnt)	1020
Vector Count Value (vcnt)	1022
Exponent Register	1024
Configuration Registers	1026
Vector Unit vregA and VregB Registers	1028
MAU state	1032
Pipeline Registers (Old values of potentially unstable scalar registers)	1034

1000 ↗

Figure 10





*Figure 11*

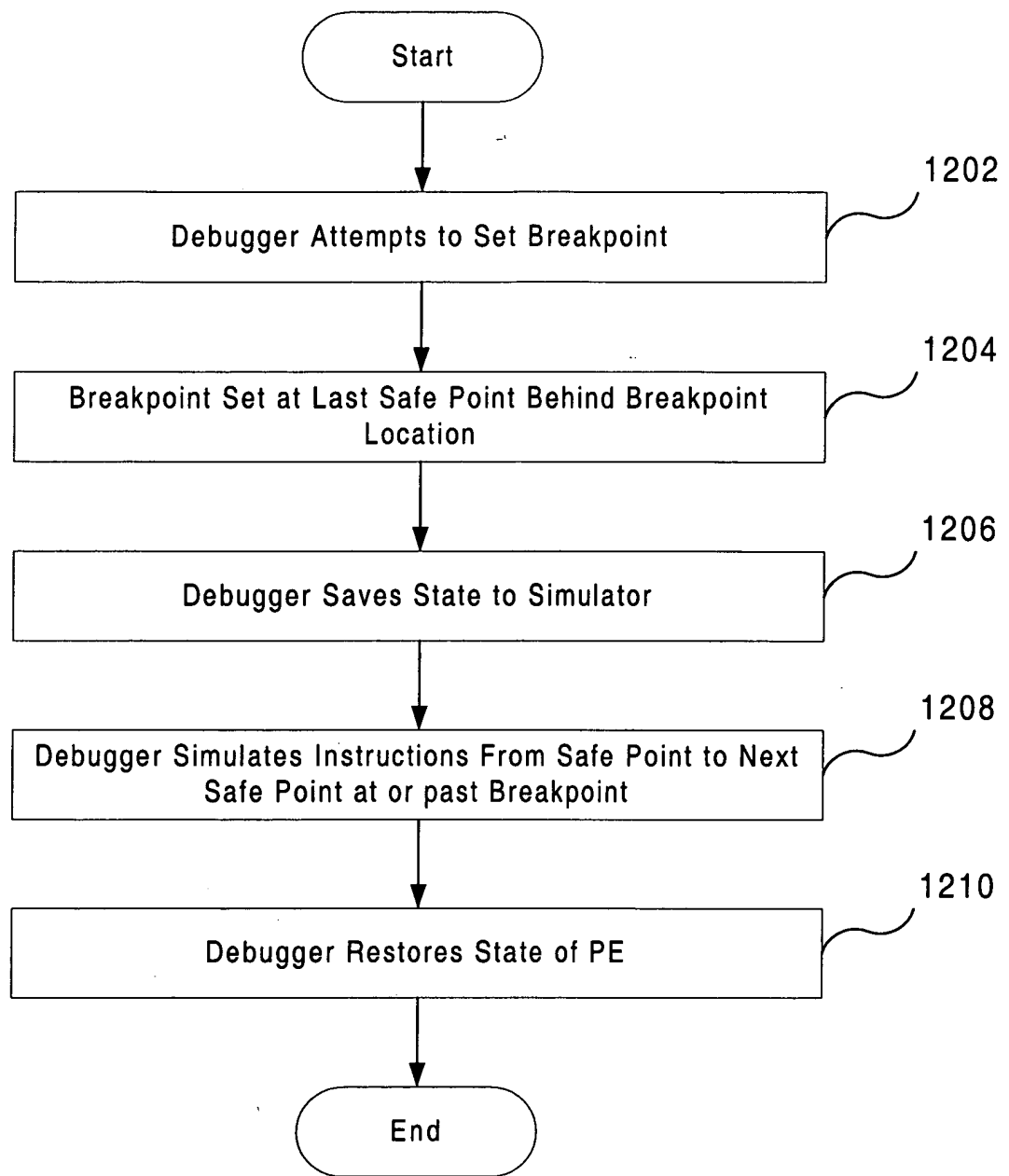


Figure 12

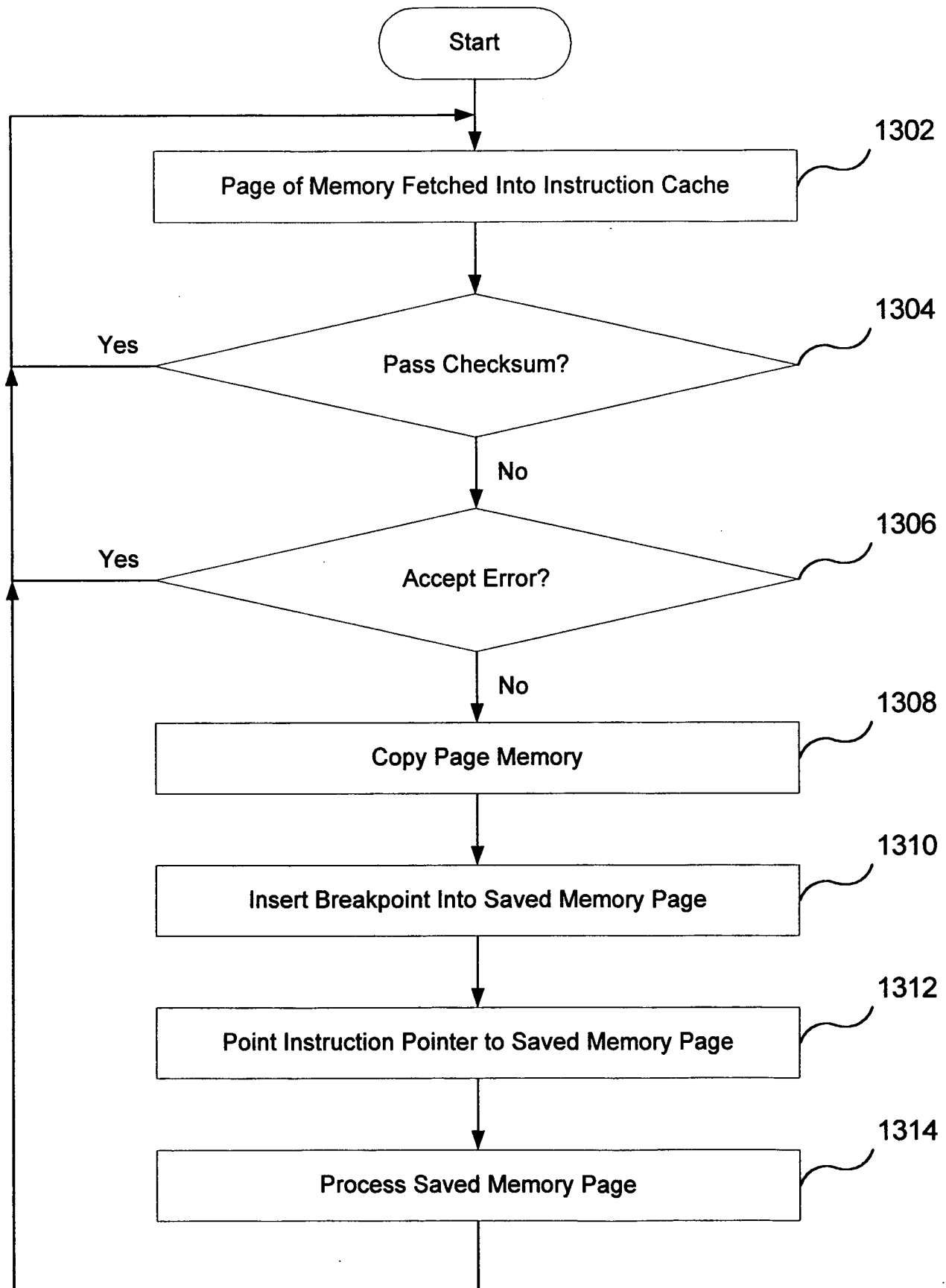


Figure 13